REMARKS

The claims are claims 1 to 5 and 8 to 12.

Claim 5 is amended. Claim 7 is canceled. Claim 5 is amended into independent form incorporating all the limitations of its base claim 1.

Claims 1 to 4, 6 and 8 to 12 were rejected under 35 U.S.C. 102(b) as anticipated by Moyer et al U.S. Patent No. 5,375,216.

Claims 1 and 8 recite subject matter not anticipated by Moyer et al. Claim 1 recites "a first requestor," "a second requestor circuit" and "access mode circuitry for indicating at least a first access mode and a second access mode." Claim 8 recites "sharing access to the memory circuit between the plurality of requestor circuits when the digital system is in a first mode of operation" and "limiting access to the first portion of memory circuit to only a first requestor of the plurality of requestors when the digital system is in a second mode of operation." Thus claims 1 and 8 recite both plural requestor circuits and plural modes. The OFFICE ACTION states that Moyer et al discloses plural requestor circuits but fails to indicate where these are disclosed. The Applicants respectfully submit that Moyer et al discloses only a single requestor circuit execution unit 42. Moyer et al states at column 1, lines 21 to 28:

> "In most data processors, two levels of privilege are provided to control access to memory, cache or otherwise, during external bus transactions and to control operation of the data processor. A supervisor mode provides the highest level of privilege. When in supervisor mode, the data processor may access memory designated for both the supervisor mode and a user mode of operation."

Reference to "the data processor" indicates this is singular. Moyer et al states at column 1, lines 43 to 49:

"For example, in the MC88100 RISC processor available from Motorola, Inc. of Austin, Tex., four instructions are accessible only in the supervisor mode of operation. Three of these instructions execute read/write accesses to a register which may only be accessed when the data processor is in a supervisor mode of operation."

Again reference to "the data processor" implies the singular. Moyer et al states at column 1, lines 52 to 54:

"If a memory, register, or instruction specified for use only in supervisor mode, is accessed when the data processor is in user mode, an exception may occur."

With plural references to data processor in the singular and no references to plural data processors, the Applicants respectfully submit that Moyer et al fails to teach the plural requestor circuits recited in claims 1 and 8. Accordingly, claims 1 and 8 are allowable over Moyer et al.

Claims 1 and 8 recite further subject matter not anticipated by Moyer et al. Claim 1 recites "the selection circuit being operable to select a first portion of the memory circuit in response to the size parameter when the access mode circuitry indicates the second access mode, wherein only the first portion of the memory circuit is operable for exclusive access by the first requestor when the access mode circuitry indicates the second access mode." Claim 8 recites "selecting a first portion of the memory circuit...such that a second portion of the memory circuit is not selected." The OFFICE ACTION cites column 10, lines 55 to 59 of Moyer et al as anticipating this subject matter. This portion of Moyer et al states:

"The SIZE signal indicates whether a memory access should be in byte, halfword, word, or double word increments. The

SIZE signal is typically encoded in the instruction opcode provided by instruction cache unit 16."

The Applicants respectfully submit that this portion of Moyer et al discloses the data size of data movement "word increments" and not portions of memory as recited in claims 1 and 8. Note especially that a memory size of a byte, a halfword, a word or a double word would be impractical to support the data accesses recited in claims 1 and 8. However, such data accesses could easily be made in "word increments" of a byte, a halfword, a word or a double word as recited in Moyer et al. Accordingly, claims 1 and 8 are not anticipated by Moyer et al.

Claims 1 and 8 recite further subject matter not anticipated by Moyer et al. Claim 1 recites "a size register for holding a size parameter coupled to the selection circuit." Claim 8 recites "a size parameter stored in a register." Thus these claims require the size parameter to be stored in a register. In contrast, the portion of Moyer et al cited in the OFFICE ACTION (quoted above) recites "The SIZE signal is typically encoded in the instruction opcode provided by instruction cache unit 16." The Applicants respectfully submit that encoding the SIZE signal in an instruction opcode does not make obvious storing this parameter in a register. Accordingly, claims 1 and 8 are not anticipated by Moyer et al.

Claims 2 and 10 recite subject matter not anticipated by Moyer et al. Claim 2 recites "wherein a second portion of the memory circuit not selected in response to the size parameter is operable to be in a low power mode when the access mode circuitry indicates the second access mode." Claim 10 recites "placing the second portion of the memory circuit in a low power mode when the digital system is in the second mode of operation." The OFFICE ACTION states at page 4, lines 9 to 11:

"said second portion would inherently placed in low power mode as it is not being addressed and the location pertaining to the second portion is not activated"

This Moyer et al fails to teach that any portion of memory is powered differently based upon the mode. If the Examiner's reasoning is to be believed, then the user memory would also be in a low power state if it is not currently being accessed. The Applicants respectfully submit that the recitations of claims 2 and 10 quoted above mean more than that the memory portion is not currently being accessed. Accordingly, claims 2 and 10 are not anticipated by Moyer et al.

Claim 6 recites subject matter not anticipated by Moyer et al. Claim 6 recites "the second requester circuit is direct memory access circuit channel controller." The Applicants respectfully submit that Moyer et al fails to teach a direct memory access channel controller. In addition, the OFFICE ACTION fails to allege that Moyer et al teaches such an element. Accordingly, claim 6 is not anticipated by Moyer et al.

Claim 12 recites subject matter not anticipated by Moyer et al. Claim 12 recites "storing a different size parameter in the register, such that the step of selecting results in a first portion having a different size in response to the different size parameter." As noted above, Moyer et al teaches that the SIZE parameter is "encoded in the instruction opcode." The Applicants respectfully submit that this teaching of Moyer et al negates any inference that the size parameter can be changed by writing to a register as recited in claim 12. Further, the OFFICE ACTION fails to allege that Moyer et al teaches this subject matter. Accordingly, claim 12 is not anticipated by Moyer et al.

Paragraph 6 of page 6 of the OFFICE ACTION stated that claim 5 would be allowable if rewritten in independent form incorporating

all limitations of its base claim. Claim 5 has been thus amended and is accordingly allowable.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

Texas Instruments Incorporated
P.O. Box 655474 M/S 3999
Dallas, Texas 75265
(972) 917-5290
Fax: (972) 917-4418

Respectfully submitted,

Robert D. Marshall, Jr.
Reg. No. 28,527